

11050 U.S. PTO  
10/026257  
2/21/01  
7C1024

PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10026257	12/21/2001	438		2812	

**\*\*APPLICANTS:** Huang Robert; Jessen Scott; Karthikeyan Subramanian; Li Joshua;  
Oladeji Isaiah; Steiner Kurt; Taylor Joseph;

**\*\*CONTINUING DATA VERIFIED:**

**\*\* FOREIGN APPLICATIONS VERIFIED:**

PG-PUB DO NOT PUBLISH ☐

RESCIND ☐

Foreign priority claimed ☐ yes ☐ no

35 USC 119 conditions met ☐ yes ☐ no

Verified and Acknowledged Examiners's initials

ATTORNEY DOCKET NO

Huang 3-8-3-2-2-25-5/7590

**TITLE :** Mask layer and dual damascene interconnect structure in a semiconductor device

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
Assistant Examiner		DRAWING	
ISSUE FEE		Sheets Drwg.	Figs. Drwg.
Amount Due	Date Paid	Print Fig.	
Primary Examiner		Application Examiner	
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>PREPARED FOR ISSUE</b>	
<b>WARNING:</b> The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.			

FILED WITH:

☐ DISK (CRF)

☐ CD-ROM

(Attached in pocket on right inside flap)